Performance of MOSFETs on Reactive-Ion-Etched GaN Surfaces

K. Tang, W. Huang, T. P. Chow
Center for Integrated Electronics, Rensselaer Polytechnic Institute, Troy, NY-12180, U.S.A.
Tel: +631-327-4978, Fax: +518-276-8761, e-mail: tangk2@rpi.edu

Previously, we have demonstrated GaN MOS with low interface densities (~10^{10}/cm^2-eV) and subsequent high performance long-channel enhancement-mode n-channel MOSFETs on p and n-GaN/sapphire substrates with maximum field-effect mobility of 167 cm^2/V-s and BV up to 940V and reverse blocking capability [1-3]. More resently, we reported the negative C-V shift, C-V stretch out, higher interface densities, and degraded field-effect mobility on RIE etched GaN MOS capacitors and MOSFETs. We also reported the wet etch treatment can only partially recover the dry etch introduced damages [4]. In this paper, we will focus on the subthreshold swing and field-effect mobility on dry/wet echted GaN MOSFETs and compare them with the unetched MOSFET.

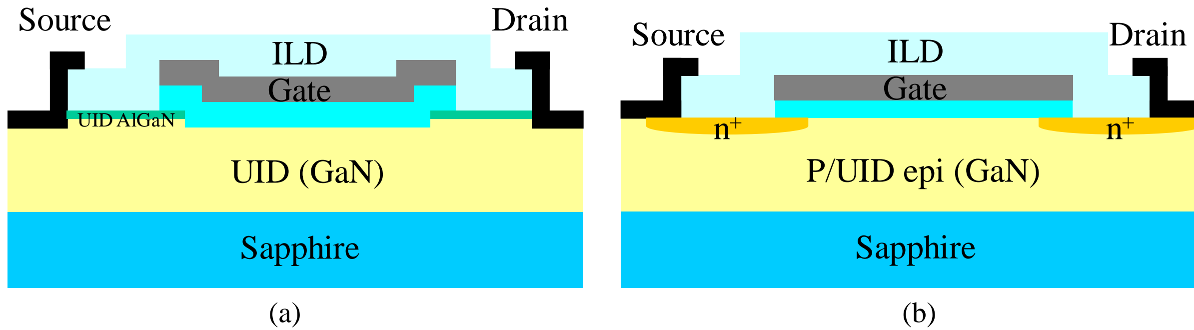
Its wide bandgap (3.4eV) and high critical electric field (3 MV/cm) make GaN attractive for high-temperature and high-voltage devices. GaN epi-RESURF and hybrid MOS-HEMT structure have better RESURF dose control, making the selective etching of GaN epi very critical to achieve both high breakdown voltage and low on-resistance. Devices with varying channel lengths were fabricated on 30nm UID $Al_{0.22}Ga_{0.78}N$ on 3µm UID GaN on sapphire substrate (MOSFET 1, 2), 0.3µm 1×10^{17}cm^{-3} n-GaN on 6µm 1×10^{16}cm^{-3} p-GaN on sapphire substrate (MOSFET 3), and 3µm UID GaN on sapphire (MOSFET 4). The schematic cross-section view and microphotograph are shown in Fig. 1 and Fig. 2 respectively. ICP etch with depths of 70nm, 50nm and 350nm were used to define gate regions for MOSFET 1, 2 and 3 respectively, followed by wet etching to remove damages from dry etching. $POCl_3$ doped polysilicon was used as gate electrode. 900°C anneal for 30 min. in N_2 was performed on 100nm gate oxide for both MOSFET 1 and 2, and 1000°C anneal for 30 min. in N_2 was performed on 100nm gate oxide for MOSFET 3 and 4. In addition, devices with 600nm field oxide as the gate insulator were also fabricated and inspected in MOSFET 1, 2 and 3. Ti/Al was deposited and annealed at 600°C for 10min. for n^+ ohmic contacts. In gate oxide devices, the subthreshold slope of MOSFET 1 (900mV/decade) and MOSFET 2 (770mV/decade) are higher than those in MOSFET 3 (300mV/decade) and MOSFET 4 (380mV/decade) (Fig. 3). Similarly, in field oxide devices, the subthreshold slope of MOSFET 1 (9V/decade) and MOSFET 2 (4.8V/decade) are higher than that in MOSFET 3 (1.5V/decade). Moreover, in gate oxide devices, a maximum field-effect mobility of 80cm^2/V-s for MOSFET 1 and 60cm^2/V-s for MOSFET 2 were extracted on long channel (L_{ch}=100 µm) devices, which are lower than the value of 120cm^2/V-s in MOSFET 3, and 170cm^2/V-s in MOSFET 4 (Fig. 4). Both of the subthreshold slope and field-effect mobility indicate the 900°C annealing condition applied in MOSFET 1, 2 process is worse than the 1000°C annealing condition applied in MOSFET 3, 4 process, which is consistent with the result of interface densities in MOS capacitors which has the lowest value with an optimized 1000°C annealing temperature [1]. In Table I, we summarized the subthreshold slope and field-effect mobility of all four MOSFETs.

In summary, we have compared the electrical characteristics of dry/wet etched and un-etched GaN MOSFETs with 900°C and 1000°C gate oxide annealing conditions. Lower subthreshold swing and higher field-effect mobility proved that the 1000°C is the optimized annealing temperature for the PECVD gate oxide in our MOSFET process.

Acknowledgement: This work was supported by NSF Center for Power Electronics Systems (EEC-9731677) and Furukawa Electric Co.

References:

1. W. Huang, T. Khan, and T. P. Chow, JEM, vol. 35, pp. 726-732, 2006.
2. W. Huang, T. Khan, and T. P. Chow, presented at ISPSD'06.
3. W. Huang and T. P. Chow, presented at ISPSD'07.
4. W. Huang, K. Tang, and T. P. Chow, to be presented at EMC'08.



(a) (b)

Fig. 1. Cross-section view of (a) MOSFET 1, 2 and (b) MOSFET 3, 4

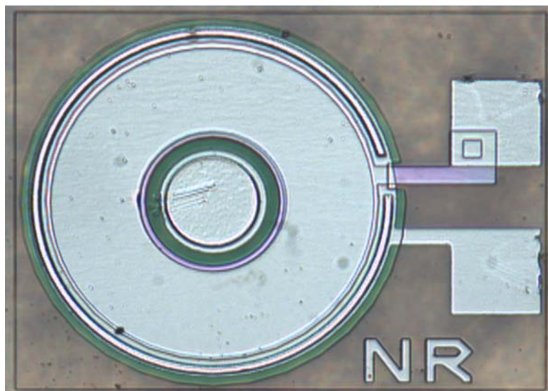


Fig. 2. Microphotograph of GaN MOSFET

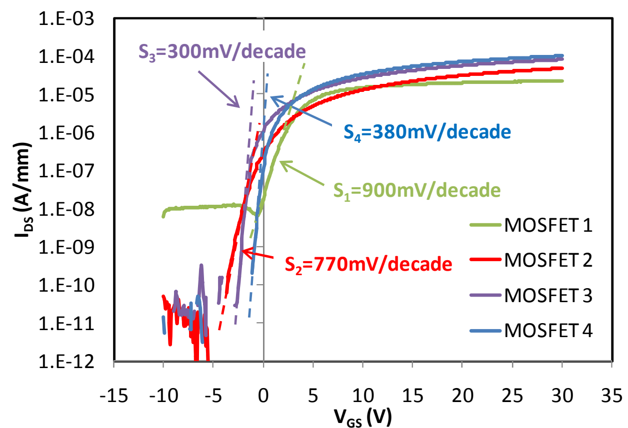


Fig. 3. Log I_D vs. V_G for MOSFETs on four different GaN surfaces

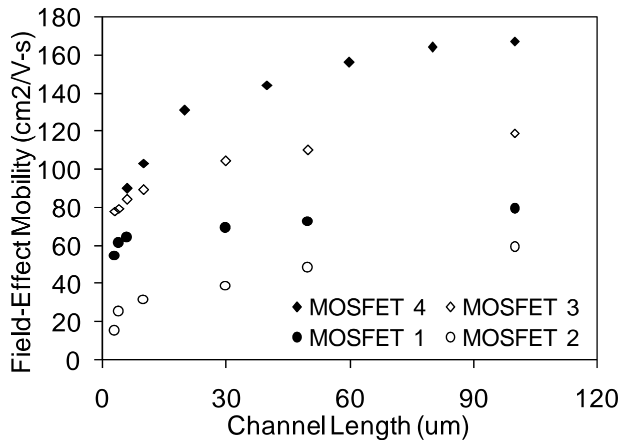


Fig. 4. Field-effect mobility with different channel length for all four MOSFETs

Table I. Subthreshold slope and field-effect mobility of MOSFETs on different GaN surfaces

	Gate Ox subthreshold	Field Ox subthreshold	Field-effect mobility
Etched MOSFET 1 (70nm)	900mV/decade	9V/decade	80cm²/V-s
Etched MOSFET 2 (50nm)	770mV/decade	4.8V/decade	60cm²/V-s
Etched MOSFET 3 EPI RESURF	300mV/decade	1.5V/decade	120cm²/V-s
Un-etched MOSFET 4	380mV/decade	N/A	170cm²/V-s